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While the **CPU** initiates the transfer by issuing a DMA command, ... The HOLD pin is used to **request** a DMA action and the HLDA pin is an output ... As mentioned above, a PCI architecture has **no** central DMA controller, unlike ISA. ... not support tri-stating the bus or **alternating** the direction of any line on the bus. ...

en.wikipedia.org/wiki/Direct\_memory\_access - Cached - Similar

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16 posts - 11 authors - Last post: Feb 26

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photo.net > ... > Nikon > Nikon Digital - Cameras and Scanners - Cached - Similar

### UCPD Berkeley | Access Control | Key Request and Fabrication Guide

**CPU** Staff review the **requests** for approval or denial and forward approved **requests** ... An **alternate** key controller, fully oriented to the department's key control system ... For lost key reports and other, **non-emergency** police services: ...

police.berkeley.edu/programsandservices/CACP/request.html - Cached

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NET is **no** exception and uses multiple threads within each worker process to .... In general, any time multiple concurrent operations **request** exclusive **access** to a ..... asynchronous is to create an **alternate** base class from which the primary ... Building asynchronous handlers to service **CPU-intensive requests** only ...

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**No** MIDlets have **access** to the device's display and input mechanisms if the user is ...

Native code can **request** the application list to be shown by sending a ... One **alternative** to giving limited **CPU access** to background applications is ...

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21 posts - 14 authors - Last post: Jan 4

Apple rejects Arrandale, **requests** GPU-less **alternative**? .... if all the other PC platform chips are designed around the **non-modified** version - that will put a ... Apple should absolutely demand a **CPU** without an integrated GPU. ... By signing up you gain complete **access** to the TechSpot community. ...

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by NR Mahapatra - 1999 - Cited by 18 - Related articles

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by UM Kuikarni - 1999 - Cited by 6 - Related articles

In **non**-cache supporting systems, each memory **access request** made by the **CPU** or other memory access devices cause the memory controller to initiate an access ...  
[www.freepatentsonline.com/5950227.html](http://www.freepatentsonline.com/5950227.html)

#### [PPT] Direct Memory Access

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In an **alternate** configuration, the DMA controller may be incorporated ... When it is ready to grant this **request**, the **CPU** sets it's Bus grant signal, BG to 1. ... **CPU**. It then writes the **no**. of bytes to be transferred into the DMA count ...  
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